REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Final Examiner's Action dated June 16, 2009, and respectfully requests reconsideration of this application in view of the foregoing amendment and following remarks.

The Applicant originally submitted Claims 1-29 in the application. In the present response, the Applicant has amended Claims 1, 26, and 19. Support for the amendment can be found, *e.g.*, on page 3, lines 2 and 3; page 5, lines 3 and 4; page 8, lines 6 to 8; page 9, lines 5 to 18; and page 11, lines 10 to 12 of the substitute specification filed on September 15, 2004. No other claims have been canceled or added. Accordingly, Claims 1-29 are currently pending in the application.

I. Rejection of Claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25-26, and 29 under 35 U.S.C. §102

Previously, the Examiner rejected Claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25-26 and 29 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,725,357 to Cousin (hereinafter "Cousin"). The Applicant respectfully disagrees.

The Examiner has acknowledged that the arguments made in the response to the previous Office Action indicate that the "control instructions" of the claimed invention are interpreted as only the instructions formatted for the general unit of Cousin. However, the Examiner then explains that he does not take this interpretation, and instead he believes that both the instructions formatted for the general unit and the instructions formatted for the address units are "control instructions".

Claim 1 has been amended to clarify the meaning of the term "control instructions", such that it is clear from the claim that the Examiner's interpretation should not be taken. In particular, Claim 1 now defines three types of instructions, those being memory access instructions having a memory

access format, control instructions having a control format, and data processing instructions having a data format. The Examiner states that the address units of Cousin are defined as executing instructions for memory accesses to a data memory – these are memory access instructions having a memory access format, not control instructions. The Examiner also states that the general unit of Cousins is defined as executing branch instructions – these are control instructions having a control format.

Once it is established that the instructions for the address units (execution units EXU3 and EXU4) in Cousin are "memory access instructions" and not "control instructions", and that only the instructions for the general unit (execution unite EXU5) constitute "control instructions having a control format", then it follows that Claim 1 of the present invention is distinguished over Cousin for the reasons given in response to the previous Office Action.

The independent claims are further distinguished from the disclosures of Cousin in that both the first and second processing channels are operable to perform memory access operations. It is clear that in Cousin the data units (EXU1 and EXU2) do not perform memory access operations. There is no motivation to modify Cousin such that the data units (EXU1 and EXU2) perform memory access operations. For at least this reason it is submitted that the combination of features in Claim 1 is not obvious from Cousin.

For completeness, and with reference to the Statement of Inventor Simon Knowles filed on June 1, 2007, we set out below the arguments presented in the response to the previous Office Action.

Cousin fails to teach at least a decode unit detecting "**if the instruction packet define (i) at least tow control instructions**", as recited in Claim 1.

It is clear from Figure 2 of Cousin and column 4, lines 32-36 of Cousin (*"According to a second instruction mode, two instructions each having a length of 32 bits are supplied to the decoder...for example W0 and W1 in the cycle0..."*) that in GP32 instruction mode a pair of instructions is passed to the decoder each cycle. This pair of instructions comprises two 32 bit instructions W0 and W1, or W2 and W3, which are decoded by the decoder 8 and sent to the relevant slots (Slot0 or Slot1). Figure 2 of Cousin also makes it clear that Instruction0 and Instruction 1 (W0 and W1) are to be executed together in the same cycle Cycle0 and Instruction2 and Instruction3 (W2 and W3) are to be executed together in the following cycle Cycle1. It is not possible, for example, for an Instruction1 and an Instruction2 to be processed together as they are from different instruction pairs executed in different cycles. **Only one of the two 32 bit instructions W0 and W1, or W2 and W3 (Instruction0 and Instruction1, or Instruction2 and Instruction3) can be a control instruction for the general unit**, which are the only "control instructions" disclosed in Cousin. This is apparent when looking at the further steps of the Cousin process as explained below.

The two 32 bit instructions Instruction0 and Instruction1 are then processed by the micro instruction generator 10. The Instruction0 in Slot0 can give rise to a micro-instruction in either or both of the two micro-slots labeled μSlot0, and the Instruction1 in Slot1 can give rise to a micro-instruction in either or both of the two micro-slots labeled μSlot1. The micro-instructions are then sent from the μSlot0 or μSlot1 to a data unit DU1, DU0, an address unit AU1, AU0, or a general unit (a control processing unit).

As stated above, a "macro-instruction" is not directed to the general unit, a macro-instruction (being either of the pairs of 32-bit instructions in a 128-bit GP32 Instruction Word) is decoded by the

decoder 8 and then processed by the micro instruction generator 10. **It is a micro-instruction which is directed to the general unit.**

Furthermore, Cousin teaches at column 6, lines 32 to 34 that "**The instructions in the first and second arrays will not both be for the general unit at the same time**" and at column 7, lines 4-6 that "**In embodiments of the invention, instructions for the general unit are not provided in both slots at the same time**". It is not possible for the left-hand pair of μSlots to contain instructions for the address unit or the general unit. The right-hand pair of μSlots may be used to supply instructions to the address units and the general unit. **However, it is not possible for both the right-hand μSlots to contain instructions for the general unit as stated explicitly in column 6, lines 32-34 and column 7, lines 4-6 of Cousin**.

Since Cousin teaches that it is not possible for both the right-hand μSlots to contain instructions for the general unit, it is not possible for the two Slots (Slot1 and Slot0, between Decoder 8 and μInstruction Generator 10 of Cousin Figure 1) to both contain Instructions destined for the General Unit. This is evident from Cousin's description of the function of the μInstruction Generator 10 and its place in the pipeline (3.32 *et seq*, 4.16 *et seq*), which makes clear that the contents of μSlot0 must come from Slot0 and the contents of μSlot1 must come from Slot1, and that Slot0 and Slot1 are processed in the same cycle (illustrated in Fig. 2 of Cousin).

Therefore, since it is not possible for both the Slots to contain instructions for the general unit at the same time, **it is not possible for any pair of 32-bit instructions passed to the decoder to comprise only instructions for the general unit only (only control instructions)**, in complete contrast with the recited limitations of independent Claim 1, 26, and 29. Therefore, in the processor disclosed by Cousin, instruction pairs such as (W1,W0) in Cousin's Fig. 2, cannot contain Control

Instructions (destined for the General Unit) in both Instruction0 (W0) and Instruction1 (W1) positions, or likewise in both Instruction2 (W2) and Instruction3 (W3) positions. Cousin teaches that the GP16 and VLIW modes have similar restrictions.

Hence, Cousin does not disclose a decode unit detecting "**if the instruction packet define (i) at least two control instructions**" as claimed in the independent claims of the subject application, since Cousin explicitly states that "***instructions for the general unit are not provided in both slots at the same time***" and consequently, a GP32 Instruction pair would not comprise instructions only for the general unit. Likewise, Cousin does not disclose "wherein when the decode unit detects that the instruction packet comprises **at least two control instructions**, said control instructions are supplied to the first processing channel for execution in program order". It is therefore submitted that independent Claims 1, 26, and 29 are novel over Cousin.

Cousin explicitly states that the instructions in the first and second arrays will not both be for the general unit at the same time (column 6, lines 32 to 34). There is no motivation for a skilled person to modify Cousin against this explicit statement such that the instructions are both for the general unit at the same time. Furthermore, there is no suggestion of how such a modification to Cousin may be achieved. It is therefore submitted that it would not be obvious to a skilled person how to modify Cousin to include the novel features recited in the independent claims of the present invention. The independent claims are therefore non-obvious over the cited prior art.

As such, Cousins does not anticipate nor render obvious independent Claims 1, 26, and 29 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102(e) rejection of Claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25-26 and 29 and allow issuance thereof.

II. Rejection of Claims 4-6, 11, 13, 15, 20, 22, 24, and 27-28 under 35 U.S.C. §103

Previously, the Examiner rejected Claims 4-6, 11, 13, 15, 20, 22, 24, and 27-28 under 35 U.S.C. §103(a) as being unpatentable over Cousin for Claim 6, 22, and 24, and Cousin in view of: U.S. Patent No. 6,880,150 to Takayama (hereinafter "Takayama") for Claims 4-5 and 11; U.S. Patent No. 5,956,518 to DeHon (hereinafter "DeHon") for Claims 13 and 15; a paper entitled "Variable Length Instruction Compression for Area Minimization," by Simonen, *et al.* (hereinafter "Simonen") for Claim 20; and a paper entitled "Structured Computer Organization," by Tanenbaum (hereinafter "Tanenbaum") for Claims 27 and 28. The Applicant respectfully disagrees.

As established above, Cousin does not render obvious independent Claims 1, 26, and 29. Takayama, DeHon, Simonen, or Tanenbaum have not been cited to correct the above-noted deficiencies of Cousin but to teach the subject matter of the above-mentioned dependent Claims. As such, Cousin or Cousin in view of Takayama, DeHon, Simonen, or Tanenbaum does not provide a *prima facie* case of obviousness for independent Claim 1, 26, and 29 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 4-6, 11, 13, 15, 20, 22, 24, and 27-28 and allow issuance thereof.

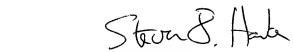
III. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-29.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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